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Design, fabrication and experimental demonstration of junction surface ion traps

D L Moehring¹, C Highstrete, D Stick, K M Fortier, R Haltli, C Tigges and M G Blain

Sandia National Laboratories, Albuquerque, NM 87185, USA

E-mail: dlmoehr@sandia.gov

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Abstract. We present the design, fabrication and experimental implementation of surface ion traps with Y-shaped junctions. The traps are designed to minimize the pseudopotential variations in the junction region at the symmetric intersection of three linear segments. We experimentally demonstrate robust linear and junction shuttling with greater than 10^6 round-trip shuttles without ion loss. By minimizing the direct line of sight between trapped ions and dielectric surfaces, negligible day-to-day and trap-to-trap variations are observed. In addition to high-fidelity single-ion shuttling, multiple-ion chains survive splitting, ion-position swapping and recombining routines. The development of two-dimensional trapping structures is an important milestone for ion-trap quantum computing and quantum simulations.

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¹ Author to whom any correspondence should be addressed.

1. Introduction

The first requirement for quantum information processing is the ability to build a ‘scalable physical system with well-characterized qubits’ [1]. In recent years, research in trapped ion quantum information has concentrated on creating scalable architectures for trapping and shuttling large numbers of ions [2–13]. Within this effort, surface-electrode ion traps are generally regarded as the most promising long-term approach due to the ability to fabricate complex trap arrays leveraging advanced semiconductor and microfabrication techniques [14–24]. Two-dimensional (2D) ion-trap geometries, such as those shown here, and ion-trap arrays are key developments for scalable implementations of ion-based quantum computation and simulation [25–27].

In this paper, we report the design, fabrication and successful testing of Y-junction surface ion traps. We demonstrate high-fidelity shuttling protocols in three different traps of two different trap designs. This includes linear and junction shuttling, splitting and recombining of ion chains, and ion reordering. The surface microtraps reported here are both reproducible and invariable. This is demonstrated by successful ion-shuttling solutions that are identical for day-to-day operation as well as for multiple congeneric traps.

2. Design and fabrication

The design principles for the traps discussed here are based in part on fabrication constraints and techniques described in our previous work [23]. These principles include minimized line of sight exposure between the ion and dielectric surfaces to ensure shielding of any trapped dielectric charge [28], and recessed bond pads to limit the projection of the wire-bond ribbons above the top surface of the trap. In addition, the top metal layout in the vicinity of the junction and the loading hole is refined with respect to radio frequency (rf) potential and other characteristics by utilizing lateral shape-modulation of electrode edges (figure 1).

As with all known junction traps, it is not possible to stabilize a trapped charge with a vanishing rf field and zero ponderomotive potential everywhere [29]. However, a suitable trade in performance characteristics can be achieved by augmenting the predicted performance using a figure of merit as a function of the electrode geometry. The trap geometries chosen here placed particular emphasis on minimizing the magnitude and slope of the equilibrium pseudopotential, particularly in the junction region, while maintaining a specified ion equilibrium height range. Resulting junction designs are shown in figures 1 and 2. The spatial features of the rf electrodes in the junction region decrease the pseudopotential barrier from greater than 1 eV for straight rf electrodes to less than 2 meV so that the ion can be transported through the junction with relatively reduced control voltages and motional heating [12] (figure 3).

Another feature of these traps is the ($70 \mu\text{m} \times 86 \mu\text{m}$) loading hole (figure 4). The presence of the loading hole, in contrast to a solid center dc electrode, also gives rise to pseudopotential barriers that can be reduced by modulating the edges of nearby rf and dc electrodes. The distance between the center of the loading hole and the center of the junction is $853 \mu\text{m}$.

Electrostatic solutions were calculated using a boundary element (BE) method to predict device performance. The BE models were created by describing electrode geometries in the form of planar polygons in three spatial dimensions in conjunction with additional meta information (i.e. ion equilibrium position, BE mesh length scale) to control model fidelity.

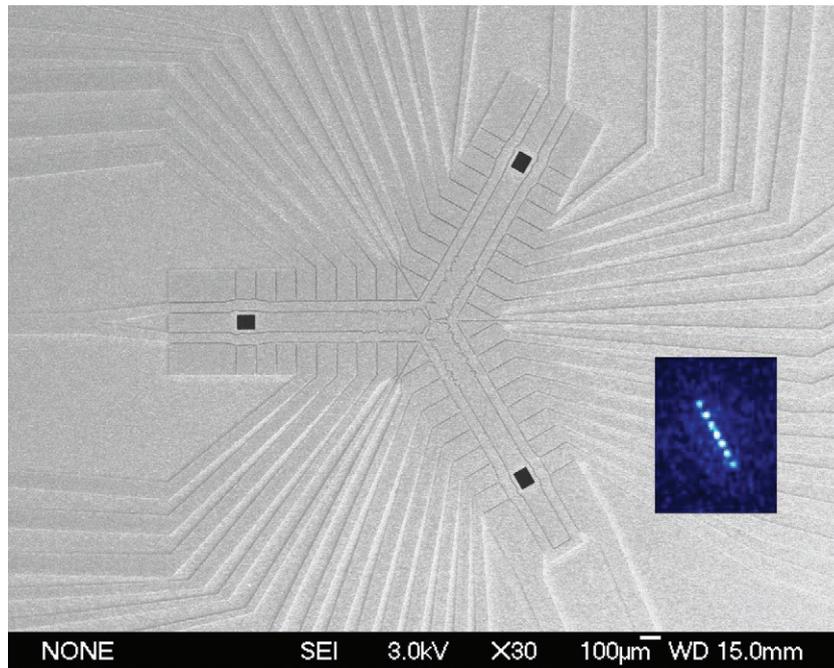


Figure 1. Scanning electron microscope (SEM) image of a Y_H -junction trap. In each trap, 47 independent dc electrodes are routed for wire bonding to the ceramic pin grid array (CPGA). The rf electrodes are $\approx 42.5 \mu\text{m}$ wide with a nominal center-to-center spacing of $\approx 142.9 \mu\text{m}$. All gaps between electrodes are $7 \mu\text{m}$. Inset: image of seven ions trapped above the loading hole. The average ion-ion spacing in this image is $\approx 3.5 \mu\text{m}$.

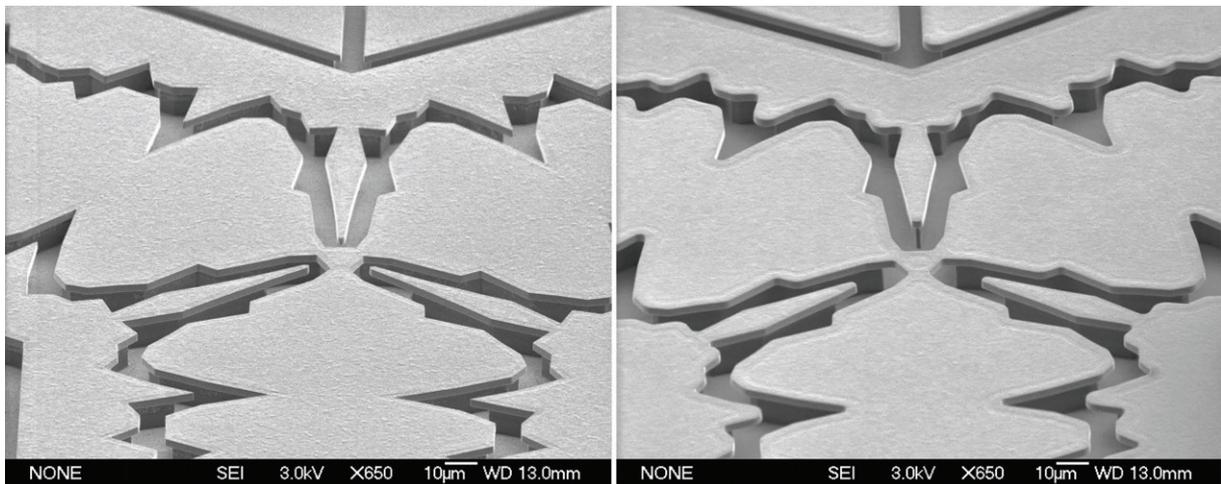


Figure 2. SEM image of the central region of the Y_H -junction trap (left) and the Y_L -junction trap (right). Note especially the sharp edges in Y_H that are rounded in Y_L .

In these models, the dielectric contribution has been ignored because these materials are always well shielded by metal. The geometries were determined by a parametric description in order to facilitate computer optimization.

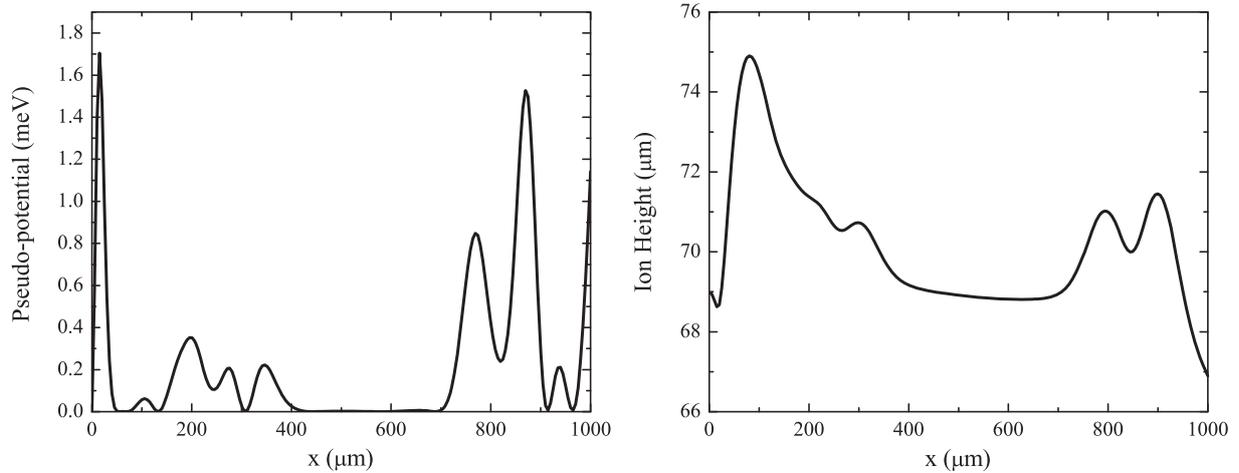


Figure 3. Left: BE simulation of the trap pseudopotential from the junction center ($x = 0 \mu\text{m}$) outward along a linear segment of the Y_H trap. The loading hole is centered at $x = 853 \mu\text{m}$. Right: height of the pseudopotential minimum above the trap surface as a function of x . The minimum of the pseudopotential follows this trajectory. The lateral position perpendicular to the trap axis does not vary significantly from zero.

Refinement of the electrode layout was accomplished by minimizing a design cost function described by parametric values for a specific geometry. This cost function was a sum of several positive semi-definite sub-cost terms that were traded by weighting coefficients. The cost functions included figures of merit for the ion height and the pseudopotential values and derivatives along the equilibrium trap axis of one arm of the Y-junction. The sub-cost values at points along the trap axis were not always treated uniformly—some points in particular were weighted differently to effect a desired outcome not achieved by solely varying the trade coefficients. For example, the ion height near the junction was reduced in cost so as to not trade so heavily against the pseudopotential minimization.

Two different trap models were fabricated and tested. Trap ‘ Y_L ’ has lower spatial frequencies on the electrode edge shapes in the junction region, whereas the second trap ‘ Y_H ’ has higher spatial frequencies (figure 2). The higher spatial frequencies in Y_H predict an overall reduction in pseudopotential barriers compared to Y_L . Two trap versions were fabricated due to a concern over the structural integrity of the cantilevered electrode segments, caused by dielectric setbacks in the high spatial-frequency regions of Y_H [23]. This concern was also addressed by using a dielectric setback of only $2 \mu\text{m}$ for Y_H , as opposed to $5 \mu\text{m}$ for Y_L . In the end, the structural integrity of the aluminum was not an issue.

3. Operation

Each fabricated ion-trap chip is packaged in a 100-pin CPGA providing electrical connections to the rf electrode and 47 independent dc electrodes. Each trap is installed in a vacuum chamber with a base pressure $\approx 5 \times 10^{-11}$ Torr following a 200°C bake for approximately 4 days. The applied dc voltages are varied between -10 V and $+10$ V using National Instruments PXI-6733 DAC cards. The applied rf voltage of ≈ 43 MHz is varied between 25 and 165 V for trapping in

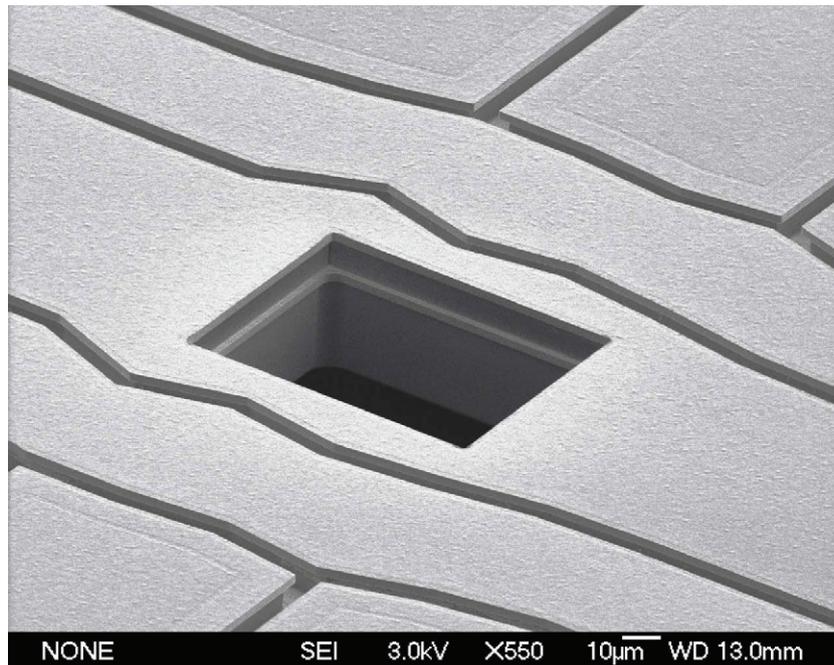


Figure 4. SEM image showing the detail of the loading hole and the modulated edges of nearby electrodes.

the loading hole and between 85 and 120 V for junction shuttling. Trapping lifetimes are several hours when the ions are Doppler cooled, and approximately 1 min without laser cooling.

Calcium ions are loaded by first generating a stream of neutral calcium atoms through the loading hole (figure 4), which are then photoionized using a resonant 423 nm laser on the $4s^1S_0 \leftrightarrow 4p^1P_1$ transition and an ionizing 375 nm laser [30]. By placing the source of the atomic beam beneath the chip, we minimize neutral atom plating on the top surface of the chip, virtually eliminating any chance of shorting adjacent trap electrodes. This is essential for consistent day-to-day trap operations [31].

The height of the ions above the top trap surface can be directly measured after shuttling the ions from the loading hole. This is accomplished by imaging the ion directly and imaging the reflected photons off the aluminum center trap electrode (figure 5). The translation of the imaging lens between the two images confirms the expected $\approx 70 \mu\text{m}$ height of the ion above the trap surface [20, 32].

In total, one Y_L trap and two Y_H traps (figure 2) were tested, with initial work performed on the Y_L trap. Here, trapping and linear shuttling tests were completed as in [23] with greater than 10^5 linear shuttles without ion loss. Junction shuttling was also tested in the Y_L trap, and despite the lower spatial frequency electrode variations, we performed 10^6 round-trip shuttles without ion loss. In a given round trip, the ion traveled up each leg of the Y-junction by $\approx 30 \mu\text{m}$, resulting in a total of 3×10^6 passes through the junction.

Following these initial successes, testing began in two congeneric Y_H traps in two independent test systems. As the Y_H trap design differs from Y_L only in the junction region, successful loading and linear shuttling voltage solutions used for Y_L were demonstrated to work also in each Y_H trap. In contrast, voltage solutions for ion transfer through the modified junction electrodes required a new shuttling routine. Interestingly, successful junction shuttling

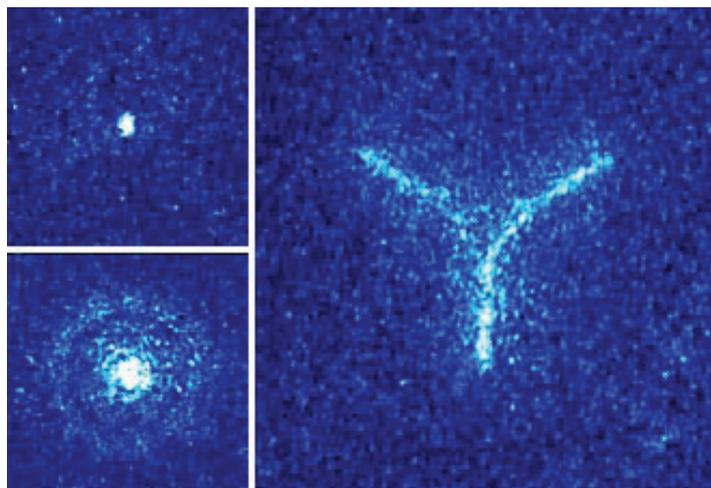


Figure 5. Left: direct image of the ion (upper) and indirect image of the ion reflected by the aluminum trap surface (lower). Right: elapsed-time image of an ion shuttling $\approx 40 \mu\text{m}$ up each arm in a Y_H trap. This 10 s image captures $\approx 40\,000$ round-trip junction shuttles. Rather than shuttling into the exact center of the junction, the ions are intentionally steered along a smooth path between the linear sections.

was observed in each Y_H trap with a voltage-solution modification consisting of a -0.5 V adjustment on only the center electrode^{2,3}.

Multiple ions were also shuttled with these solutions from the loading hole, thrice through the junction, and back to the loading hole. One round trip reverses the order of ions within the linear chain; however, this is difficult to prove unequivocally as all ions were the same isotope ($^{40}\text{Ca}^+$). All of the above-mentioned tests utilized high-degree-of-freedom voltage solutions, which used up to 25 dc electrodes at a given time for linear shuttling and 35 dc electrodes for junction shuttling.

After success with the high-degree-of-freedom solutions, we tested voltage solutions with a reduced number of dc electrodes. This is convenient for parallel shuttling of ions in multiple harmonic wells with minimal cross-talk. It is also convenient to use voltage shuttling solutions with a constant center dc electrode (see footnote 2). With solutions utilizing only the nearest 7 dc electrodes at any one time in the linear regions and the central 13 dc electrodes in the junction region (including the center electrode), ions were shuttled to all functional regions of each trap. Ions survive these routines with or without Doppler cooling during shuttling.

As in the Y_L trap, a single ion in a Y_H trap successfully completed 10^6 round-trip shuttles around the junction without ion loss. With the ion moving $40 \mu\text{m}$ up each arm, 10^6 shuttles took about 4 min, whereas moving $250 \mu\text{m}$ up each arm took about 24 min. In the latter case, the ion traveled a total distance of 1.5 km at an average speed of 1 m s^{-1} . Utilizing Doppler cooling during the junction shuttling routine, the emission of photons from the ion resulted in the trace of

² The center dc electrode is directly underneath the ion and extends the entire trapping region. A voltage applied to this electrode is applied to all regions of the trap.

³ Reverse compatibilities of the solutions tested in the Y_H trap were not tested in the Y_L trap as it was no longer installed in a test setup.

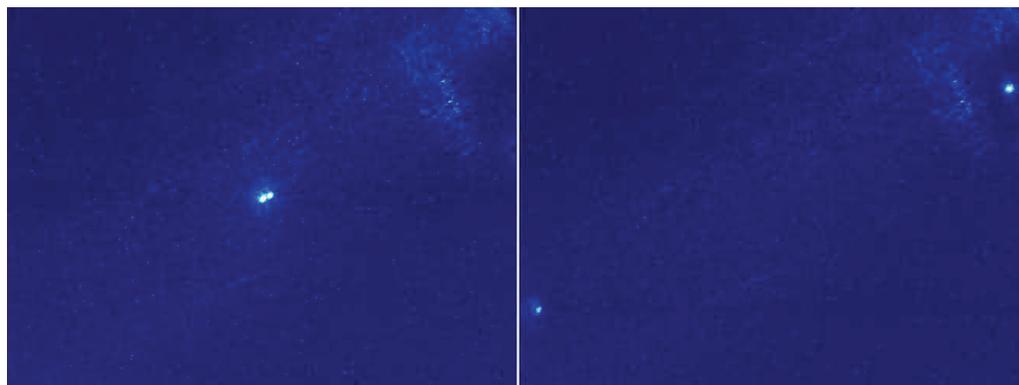


Figure 6. Left: ions within the same harmonic well separated by approximately $6\ \mu\text{m}$. Right: ions separated by four electrodes (approximately $370\ \mu\text{m}$). The splitting and recombining of two ions was explicitly observed hundreds of times without error.

the ion path shown in figure 5. Voltage solutions successful in one Y_H trap were also successful in a second identically constructed Y_H trap, even though the two traps were tested in different vacuum chambers with independent rf and dc voltage sources—only lasers were shared between the two setups. These solutions have been successfully used without modification for over six months.

Finally, complex shuttling routines were implemented for multiple ions in several locations on a given trap. For instance, three ions were consecutively loaded, independently shuttled into each arm of the junction, and Doppler cooled in a triangular configuration for over an hour without loss. Linear ion chains were also split and recombined as seen in figure 6. By performing independent junction shuttling between splitting and recombining, two ions were unequivocally observed to exchange position in a linear chain.

4. Conclusion

Reliable and repeatable microfabrication of complex ion-trapping structures has been demonstrated, indicating that a scalable system of trapped ions for quantum computation and quantum simulation is conceivable. By further utilizing the device design and integration capabilities of multi-layer fabrication techniques, the robust fabrication of more complex 2D and 3D trap arrays is imminent [25]. For example, multi-level metalization (up to four levels of metal) is being employed to accommodate nested trap electrodes and to minimize electrode cross-talk, thereby enabling fundamentally new trap array concepts.

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